



# Utilizing Macromodels in Floating Random Walk Based Capacitance Extraction

**Wenjian Yu**

Department of Computer Science and Technology,  
*Tsinghua University*, Beijing 100084, China

[yu-wj@tsinghua.edu.cn](mailto:yu-wj@tsinghua.edu.cn)

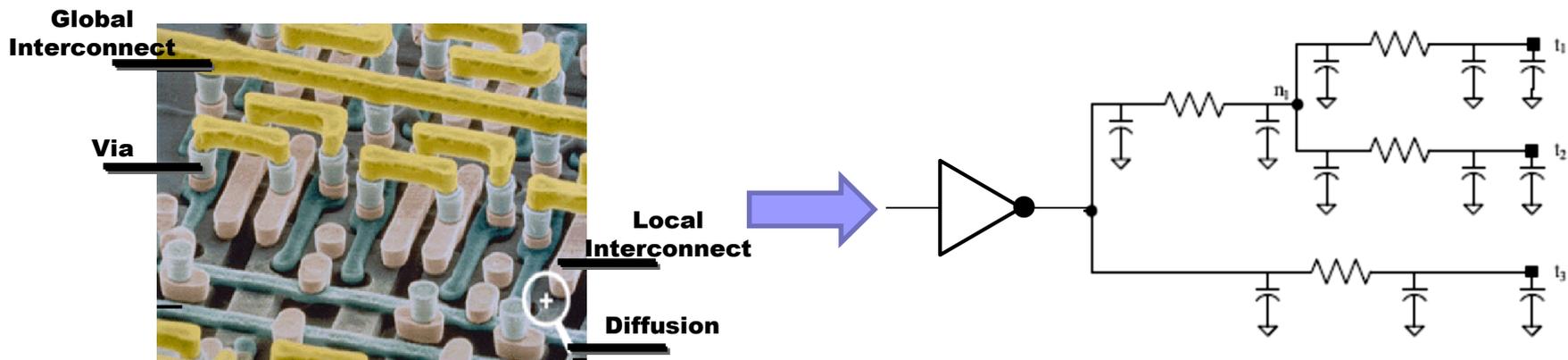
Based on the paper by W. Yu, B. Zhang, C. Zhang, H. Wang, and L. Daniel on the *Design, Automation & Test in Europe (DATE) Conference* held at Dresden, Germany in Mar. 2016.

# Outline

- **Introduction**
- **Technical Background**
- **The Macromodel-Aware Random Walk Algorithm**
- **Its Application to Capacitance Extraction Problems**
- **Conclusion**
- **References to Our Related Works**

# Introduction

- Model interconnect wires in nanometer ICs
  - Signal delay on wire has dominated the circuit delay
  - Verifying delay constraints is a major task in IC design



- Capacitance extraction: calculating the capacitances
- Base stone for interconnect model and circuit verification
- More **structure complexity** and higher **accuracy demand** call for field-solver techniques for capacitance extraction

# Introduction

- Field-solver capacitance extraction  $\begin{cases} \nabla^2 \phi = 0 \\ C_{ij} = \int_{\Gamma_j} \frac{\partial \phi}{\partial \vec{n}} ds \end{cases}$

Raphael

- Finite difference/finite element method

- Stable, versatile; slow

- Boundary element method

- Fast; surface discretization

$$Ax = b$$

FastCap, Act3D  
QBEM/HBBEM

- Floating random walk method

QuickCap/Rapid3D, RWCap

- A variant of GFFP-WOS method; discretization-free

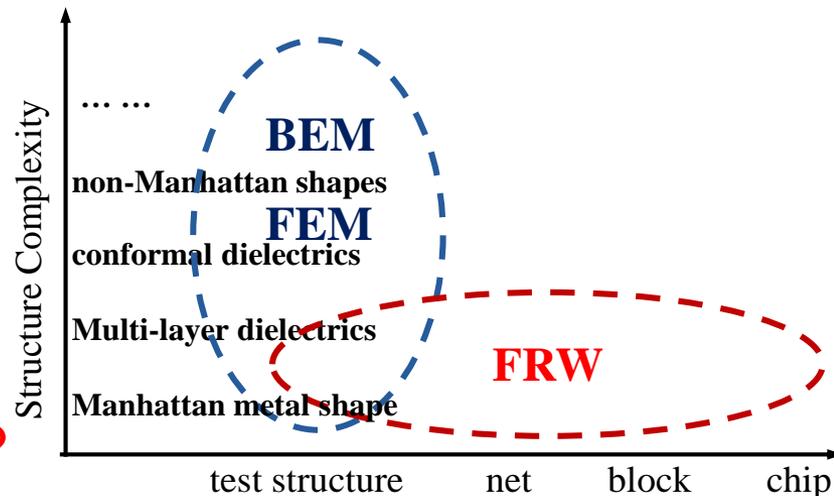
- Less memory; scalability

- Stochastic error; controllable

- Reliable accuracy

- Easy for parallelization

- How to extend the capability of FRW for complex structure?

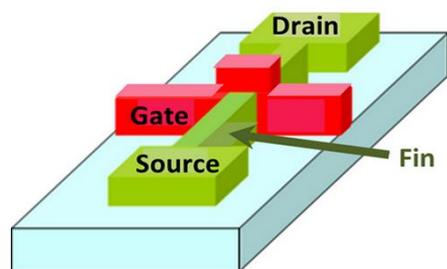


# Introduction

- The challenge from encrypting the structure information

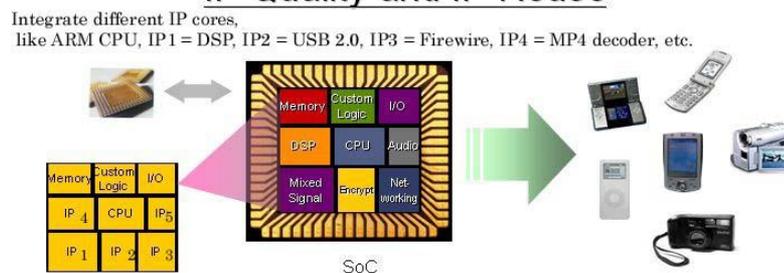
- Accurate extraction needs structure/geometry details

Advanced FinFET (foundry)



Layout of IP core (IP vendor)

IP Quality and IP Reuse



- Foundry/IP vendor need protect their trade secrets by hiding sensitive structure information → **A contradiction!**
- Intuitive solution: build a macromodel for sensitive region
  - It's recently proposed with a FDM based implementation [1]
  - The used macromodeling technique was created many years ago for reducing the runtime for large structure [2]

[1] W. Shi and W. Qiu, "Encrypted profiles for parasitic extraction," *US Patent*, 2013

[2] T. Lu, et al., "Hierarchical block boundary-element method (HBBEM): a fast field solver for 3-D capacitance extraction," *IEEE Trans. MTT*, 2004

# Introduction

- Notice: the macromodeling technique has not been utilized by the state-of-the-art FRW based capacitance solver
- The aim of this work
  - Combine macromodeling and FRW techniques, to improve the capacitance field solver for several scenarios
- **Major contributions**
  - A new random walk algorithm which utilizes the macromodel and is able to handle general 3-D layout
  - Handle the capacitance extraction with encrypted structures, while keeping the advantages of FRW method
  - We also propose to apply it to problems with complex geometry and repeated layout patterns, for extending FRW's capability and improving its runtime efficiency

# Outline

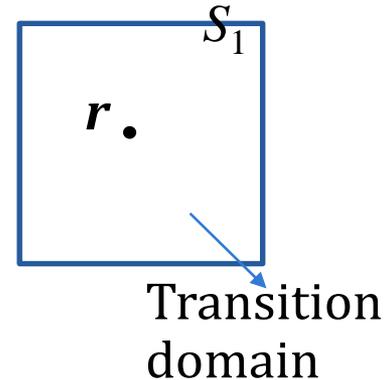
- Introduction
- **Technical Background**
- The Macromodel-Aware Random Walk Algorithm
- Its Application to Capacitance Extraction Problems
- Conclusion
- References to Our Related Works

# Technical Background – FRW method

- Integral formula for electric potential

$$\phi(\mathbf{r}) = \oint_{S_1} P_1(\mathbf{r}, \mathbf{r}^{(1)}) \phi(\mathbf{r}^{(1)}) d\mathbf{r}^{(1)}$$

Surface Green's function  $P_1$  can be regarded as a probability density function



- Monte Carlo method:  $\phi(\mathbf{r}) = \frac{1}{M} \sum_{m=1}^M \phi_m$

$\phi_m$  is the potential of a point on  $S_1$ , randomly sampled with  $P_1$

- How to do if  $\phi_m$  is unknown? expand the integral recursively

$$\phi(\mathbf{r}) = \oint_{S_1} P_1(\mathbf{r}, \mathbf{r}^{(1)}) \oint_{S_2} P_1(\mathbf{r}^{(1)}, \mathbf{r}^{(2)}) \dots \oint_{S_k} P_1(\mathbf{r}^{(k-1)}, \mathbf{r}^{(k)}) \phi(\mathbf{r}^{(k)}) d\mathbf{r}^{(k)} \dots d\mathbf{r}^{(2)} d\mathbf{r}^{(1)}$$

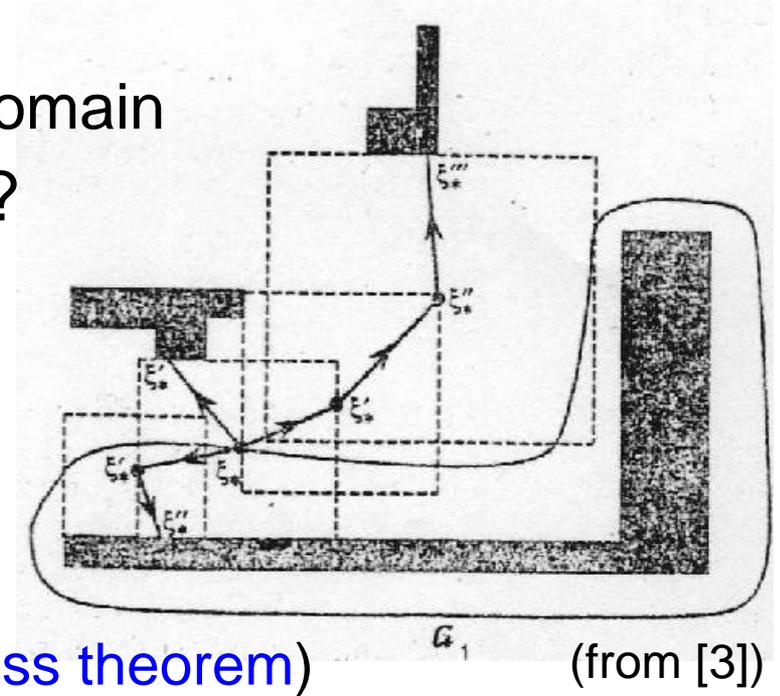
This spatial sampling procedure is called **floating random walk**

# Technical Background – FRW method

- A 2-D example with 3 walks
  - Use maximal cube transition domain
- How to calculate capacitances?

$$\begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{12} & C_{22} & C_{23} \\ C_{13} & C_{23} & C_{33} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} Q_1 \\ Q_2 \\ Q_3 \end{bmatrix}$$

$$\Rightarrow Q_1 = C_{11}V_1 + C_{12}V_2 + C_{13}V_3$$



Integral for calculating charge (Gauss theorem) (from [3])

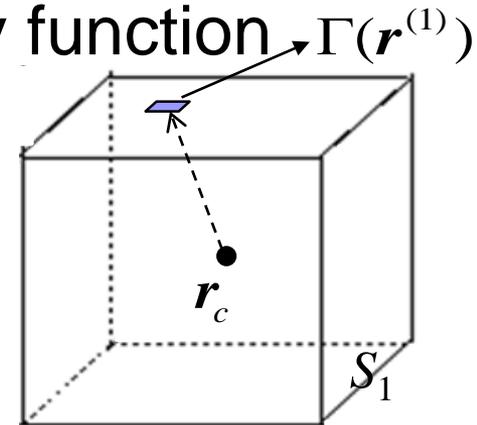
$$\begin{aligned} \underline{Q}_1 &= \oint_{G_1} F(\mathbf{r}) \cdot \hat{n} \cdot \nabla \phi(\mathbf{r}) d\mathbf{r} = \oint_{G_1} F(\mathbf{r}) \cdot \hat{n} \cdot \nabla \oint_{S_1} P_1(\mathbf{r}, \mathbf{r}^{(1)}) \phi(\mathbf{r}^{(1)}) d\mathbf{r}^{(1)} d\mathbf{r} \\ &= \oint_{G_1} F(\mathbf{r}) g \oint_{S_1} P_1(\mathbf{r}, \mathbf{r}^{(1)}) \phi(\mathbf{r}^{(1)}) \omega(\mathbf{r}, \mathbf{r}^{(1)}) d\mathbf{r}^{(1)} d\mathbf{r} \end{aligned}$$

weight value, estimate of  $C_{11}, C_{12}, C_{13}$  coefficients

[3] Y. Le Coz, et al., "A stochastic algorithm for high speed capacitance extraction in integrated circuits," *Solid-State Electronics*, 1992

# Technical Background – FRW method

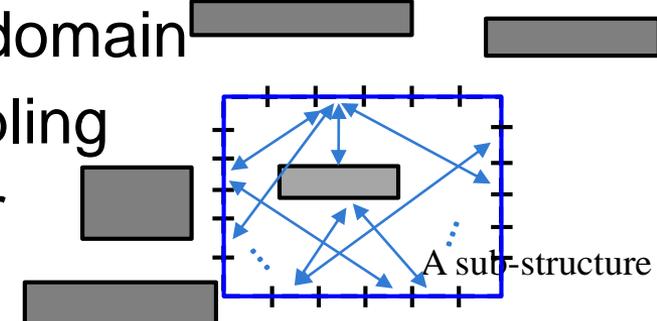
- Make random sampling with  $P_1$  probability function  $\Gamma(\mathbf{r}^{(1)})$ 
  - Available for cube transition domain
  - Pre-calculate the probabilities from center to surface panels (GFT)
  - $\omega(\mathbf{r}, \mathbf{r}^{(1)})$  is also pre-calculated (WVT)
- Keys of fast FRW algorithm for Manhattan geometry
  - GFT/WVTs for cubic transition domain are critical for performing fast sampling
  - Large probability to terminate a walk; easy to design a spatial structure for fast calculation of distance [4]
  - Techniques for handling multiple planar dielectrics
- Runtime of FRW:  $T_{total} = N_{walk} \cdot N_{hop} \cdot T_{hop}$



[4] C. Zhang, et al., "Efficient space management techniques for large-scale interconnect capacitance extraction with floating random walks," *IEEE Trans. CAD*, 2013

# Technical Background – Macromodeling

- The idea of macromodel for capacitance extraction

- Built for a sub-structure in problem domain 
- A matrix reflecting electrostatic coupling
- Built with FDM or BEM, originally for global hierarchical extraction [5][2]

- Two different definitions

- Boundary potential-flux matrix (BPFM):  $Au = \tilde{q}$   
 $u$  and  $\tilde{q}$  are vectors of potential and normal electric field intensity on the boundary elements. [5][2]
- Boundary potential-charge matrix (BPCM):  $Cu = q$   
 $q$  is vector of electric charge. Called Markov transition matrix [6]

- We use BPCM  $C$   Capacitance matrix for a closed-domain

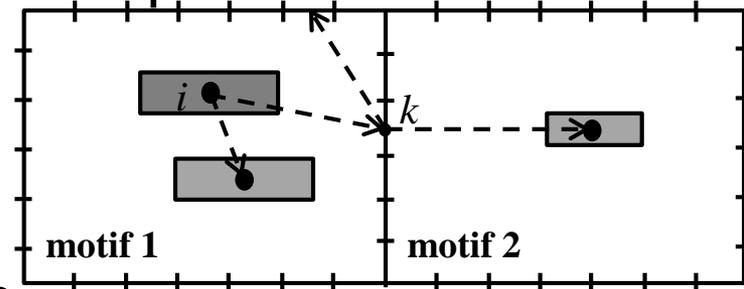
[5] E. Dengi and R. Rohrer, "Boundary element method macromodels for 2-D hierarchical capacitance extraction," *DAC*, 1998

[2] T. Lu, et al., "Hierarchical block boundary-element method (HBBEM): a fast field solver for 3-D capacitance extraction," *IEEE Trans. MTT*, 2004

[6] T. El-Moselhy, et al., "A markov chain based hierarchical algorithm for fabric-aware capacitance extraction," *IEEE T-AP*, 2010

# Technical Background – Markov chain RW

- The fabric-aware capacitance extraction problem [6]
  - Simulated structure: a combination of predefined motifs
  - Motif positions topologically vary
  - A hierarchical random walk method pre-calculates BPCM for each motif, and then performs Markov chain RWs among boundary elements/conductors



$$Q_i = \left(-c_{ii}^{(1)}\right) \sum_{j=1, j \neq i}^{N_1} \left[ \frac{c_{ij}^{(1)}}{c_{ii}^{(1)}} \right] U_j^{(1)}$$

$c^{(1)}$  ~ a capacitance matrix  
they are probabilities for random transition

- On the interface of motifs

$$U_k = \sum_{j=1, j \neq k}^{N_1} \left[ \frac{-c_{kj}^{(1)}}{c_{kk}^{(1)} + c_{kk}^{(2)}} \right] U_j^{(1)} + \sum_{j=1, j \neq k}^{N_2} \left[ \frac{-c_{kj}^{(2)}}{c_{kk}^{(1)} + c_{kk}^{(2)}} \right] U_j^{(2)}$$

*No geometry computation. So, MCRW runs faster than FRW !*

# Outline

- Introduction
- Technical Background
- **The Macromodel-Aware Random Walk Algorithm**
- Its Application to Capacitance Extraction Problems
- Conclusion
- References to Our Related Works

# Macromodel-Aware Random Walk Algorithm

- A general structure partially described by macromodels

- MCRW doesn't work

- The new algorithm

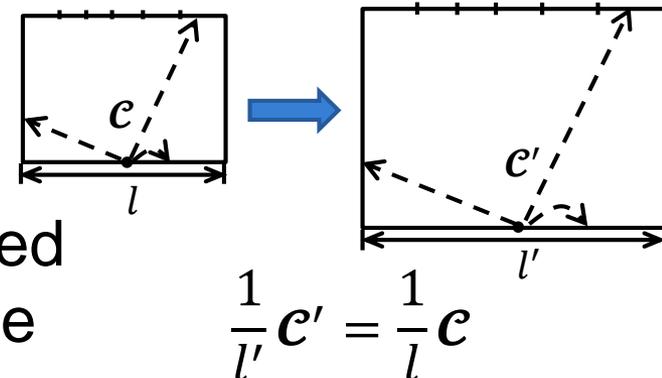
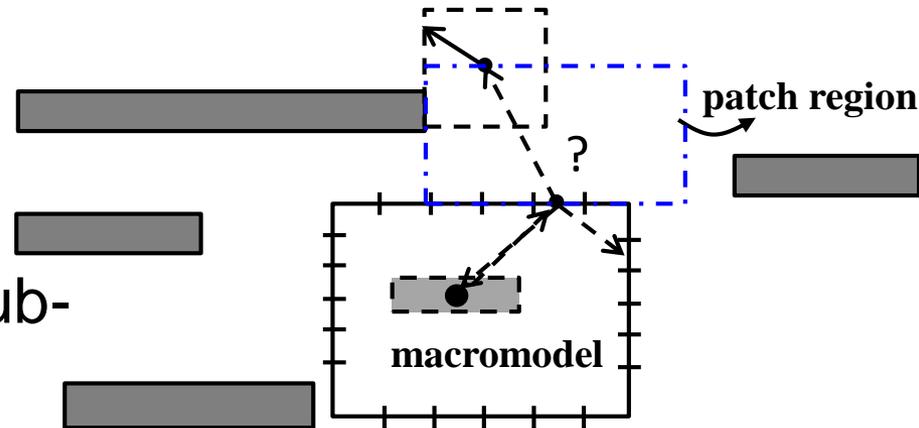
- **Idea:** Use a **patch region** to combine MCRW for a sub-structure with macromodel

- + FRW for the structure elsewhere

- If we have the macromodel for the patch, MCRW works for sub-structure's boundary point

- Then, if the walk position is out of sub-structure, the FRW is feasible

- This blank patch region can be scaled in size, with its macromodel reusable

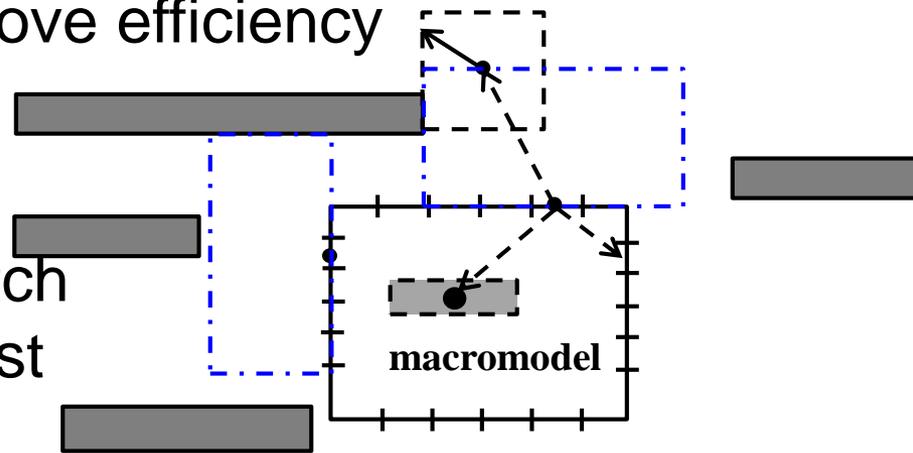


# Macromodel-Aware Random Walk Algorithm

- The benefits of this new algorithm
  - Solve the structure encryption problem in FRW-based extr.
  - Extend capability and improve efficiency

- Some details

- Patch region = half a cube
- Easy to find the largest patch (similar to finding the largest transition cube in FRW)
- Walk point always corresponds to same local index in patch's macromodel, only one row of BPCM is needed



- A new MCRW formula for the mismatched interface discretization
 
$$U_k = \sum_{j=1, j \neq k}^{N_1} \frac{\frac{-c_{kj}^{(1)}}{A_k^{(1)}}}{\frac{c_{kk}^{(1)}}{A_k^{(1)}} + \frac{c_{kk}^{(2)}}{A_k^{(2)}}} U_j^{(1)} + \sum_{j=1, j \neq k}^{N_2} \frac{\frac{c_{kj}^{(2)}}{A_k^{(2)}}}{\frac{c_{kk}^{(1)}}{A_k^{(1)}} + \frac{c_{kk}^{(2)}}{A_k^{(2)}}} U_j^{(2)}$$

# Outline

- **Introduction**
- **Technical Background**
- **The Macromodel-Aware Random Walk Algorithm**
- **Its Application to Capacitance Extraction Problems**
- **Conclusion**
- **References to Our Related Works**

# Capacitance Extraction Applications

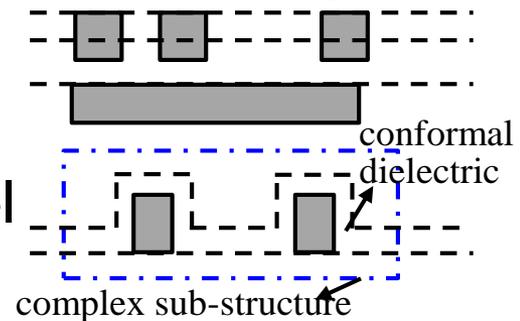
- Three kinds of applications

- Encryption of sensitive structure

- Foundry/IP vendor build macromodel for a sensitive region, avoid presenting its details to EDA vendor/IC designer
- Memory cost depends on the quantity/size of such regions

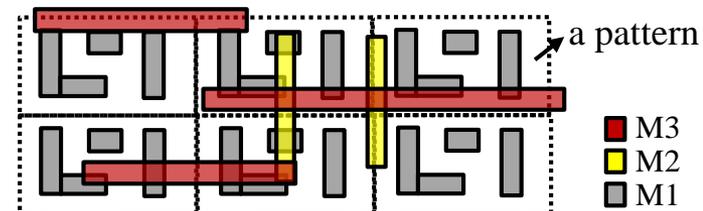
- Handling complex sub-structure

- Select a sub-region including complex geometry feature, and make macromodel
- Extend the capability of FRW method
- Useful for digital circuit with minor complex features



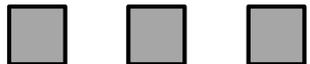
- Circuit w/ repeated layout patterns

- Memory IC or FPGA
- Reduce memory for storing layout
- Accelerate the capacitance extraction



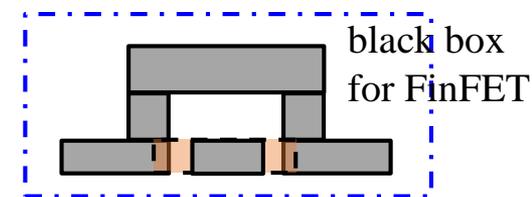
# Numerical Results with 3-D Test Cases

## ■ Experiment setup

- All random walk programs terminate with 0.5% 1- $\sigma$  error
- Macromodels are built with BEM; data size for the patch is 162KB/1.5MB for single/multi-dielectric cases 
- Serial computing on Xeon 2.0GHz CPU 

## ■ Encryption of sensitive structure

- **Case 1:** 3x3 crossover above a FinFET
- **Case 2:** two FinFET black boxes



Test case	RWCap2 <sup>[4]</sup>				The proposed method				
	N <sub>walk</sub>	N <sub>hop</sub>	C(aF)	time(s)	N <sub>walk</sub>	N <sub>hop</sub>	C(aF)	Err(%)	time(s)
1	351K	39.5	21.39	3.27	292K	30.8	21.6	1.0	1.97
2	161K	37.4	21.86	1.47	125K	26.5	22.06	0.9	0.71

~ 2X speedup

8.2MB data size for macromodeling the FinFET black box

[4] C. Zhang, et al., "Efficient space management techniques for large-scale interconnect capacitance extraction with floating random walks," *IEEE Trans. CAD*, 2013. <http://numbda.cs.tsinghua.edu.cn/rwcap.htm>

# Numerical Results with 3-D Test Cases

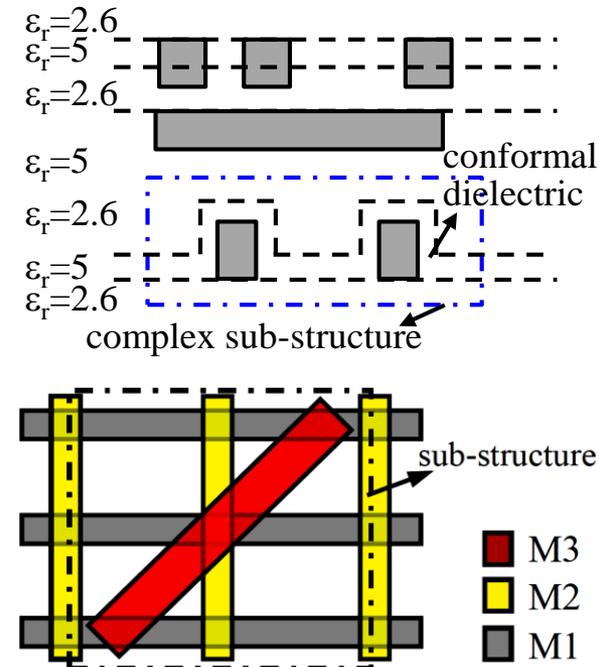
- Handling complex sub-structure

- Case 3: include conformal dielectric
- Case 4: a 45°-angle bevel wire above a 3x3 crossover
- Set a mid-layer conductor as master

Test case	Raphael	The proposed method				
	C(aF)	$N_{walk}$	$N_{hop}$	C(aF)	Err(%)	time(s)
3	66.14	370K	39.2	67.23	1.6	3.86
4	47.68	152K	20.0	48.00	0.7	0.72

The slightly larger error for Case 3 may be caused by different outer-boundary condition in Raphael RC3

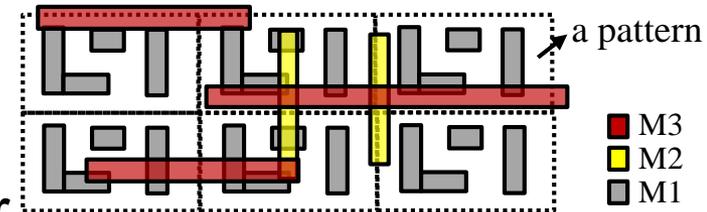
- The sub-structures in Case 3, 4 cost 7.1MB and 45MB macromodel data; building time is 2.87s and 24.1s
- Cost may be amortized for extraction w/ multiple masters



# Numerical Results with 3-D Test Cases

- Circuit with repeated layout patterns

- **Case 5:** 8x8 duplication of a structure pattern in M1 layer
- Set different conductors as master



Case 5	RWCap2 <sup>[4]</sup>				The proposed method					
master	$N_{walk}$	$N_{hop}$	C(aF)	time(s)	$N_{walk}$	$N_{hop}$	C(aF)	Err(%)	time(s)	Sp.
Con1	217K	27.7	43.31	1.63	175K	20.0	43.60	0.7	0.94	1.7
Con2	577K	14.1	5.807	2.13	8K	10.2	5.884	1.3	0.18	12
Con3	286K	35.2	3.719	2.75	16K	18.5	3.747	0.8	0.44	6

- 2.7s and 6.4MB data are needed for macromodeling
- If the master is within a cyclic pattern, the proposed method can be > 10X faster than FRW
- Markov Chain RW makes  $N_{walk}$  largely reduced

[4] C. Zhang, et al., "Efficient space management techniques for large-scale interconnect capacitance extraction with floating random walks," *IEEE Trans. CAD*, 2013. <http://numbda.cs.tsinghua.edu.cn/rwcap.htm>

# Conclusion

- **The Markov chain random walk and the floating random walk are combined to accelerate the capacitance extraction, and handle circuits including IP protected or geometry-complex sub-structures**
- **The scalable blank patch region: with it and its macromodel, we can establish a general & accurate macromodel-aware extraction algorithm**
- **It extends the capability of the state-of-the-art FRW based capacitance solver with negligible overhead**
- **It can bring over 10X speedup to the FRW based extraction for circuit with repeated layout patterns**

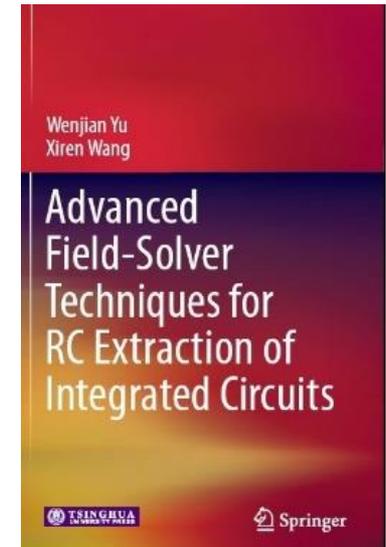
# References

## The Floating Random Walk Algorithms for Capacitance Extraction Problems in IC and FPD Design:

- W. Yu, H. Zhuang, C. Zhang, G. Hu, and Z. Liu, "RWCap: A floating random walk solver for 3-D capacitance extraction of VLSI interconnects," *IEEE Trans. Computer-Aided Design*, 32(3): 353-366, 2013
- C. Zhang and W. Yu, "Efficient space management techniques for large-scale interconnect capacitance extraction with floating random walks," *IEEE Trans. Computer-Aided Design*, 32(10): 1633-1637, 2013
- C. Zhang, W. Yu, Q. Wang, and Y. Shi, "Random walk based capacitance extraction for 3D ICs with cylindrical inter-tier-vias," *IEEE Trans. Computer-Aided Design*, 34(12): 1977-1990, 2015
- Z. Xu, C. Zhang, and W. Yu, "Floating random walk based capacitance extraction for general non-Manhattan conductor structures," *IEEE Trans. Computer-Aided Design*, 2016
- B. Zhang, W. Yu, and C. Zhang, "Improved pre-characterization method for the random walk based capacitance extraction of multi-dielectric VLSI interconnects," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, 29(1): 21-34, 2016
- W. Yu, B. Zhang, C. Zhang, H. Wang, and L. Daniel, "Utilizing macromodels in floating random walk based capacitance extraction," in *Proc. DATE'2016*, Dresden, Germany, Mar. 2016, pp. 1225-1230. **(Best Paper Award!)**

# References

- K. Zhai, W. Yu, and H. Zhuang, “GPU-Friendly floating random walk algorithm for capacitance extraction of VLSI interconnects,” in *Proc. DATE’2013*, Grenoble, France, Mar. 2013, pp. 1661-1666.
- C. Zhang and W. Yu, "Efficient techniques for the capacitance extraction of chip-scale VLSI interconnects using floating random walk algorithm," in *Proc. ASP-DAC’2014*, Singapore, Jan. 2014, pp. 756-761.
- Z. Xu, W. Yu, C. Zhang, B. Zhang, M. Lu, and M. Mascagni, "A parallel random walk solver for the capacitance calculation problem in touchscreen design," in *Proc. GLSVLSI’2016*, Boston, MA, May 2016, 99-104.
- Wenjian Yu and Xiren Wang,  
*Advanced Field-Solver Techniques for RC Extraction of Integrated Circuits*,  
Springer Inc., May 2014 (246 pages)
- My Homepage:
- <http://numbda.cs.tsinghua.edu.cn>



*Thank You !*

