Utilizing Macromodels in Floating Random Walk Based Capacitance Extraction

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Outline

- Introduction
- Technical Background
- The Macromodel-Aware Random Walk Algorithm
- Its Application to Capacitance Extraction Problems
- Conclusion
- References to Our Related Works
Introduction

- Model interconnect wires in nanometer ICs
  - Signal delay on wire has dominated the circuit delay
  - Verifying delay constraints is a major task in IC design

- Capacitance extraction: calculating the capacitances
- Base stone for interconnect model and circuit verification
- More structure complexity and higher accuracy demand call for field-solver techniques for capacitance extraction
Introduction

- Field-solver capacitance extraction
  - Finite difference/finite element method
    - Stable, versatile; slow
  - Boundary element method
    - Fast; surface discretization
  - Floating random walk method
    - A variant of GFFP-WOS method; discretization-free
    - Less memory; scalability
    - Stochastic error; controllable
    - Reliable accuracy
    - Easy for parallelization
- How to extend the capability of FRW for complex structure?

\[
\begin{aligned}
\nabla^2 \phi &= 0 \\
C_{ij} &= \int_{\Gamma_j} \frac{\partial \phi}{\partial \hat{n}} ds
\end{aligned}
\]

Raphael

FastCap, Act3D, QBEM/HBBEM

QuickCap/Rapid3D, RWCap
Introduction

- The challenge from encrypting the structure information
  - Accurate extraction needs structure/geometry details
  - Advanced FinFET (foundry)
  - Layout of IP core (IP vendor)

- Foundry/IP vendor need protect their trade secrets by hiding sensitive structure information → A contradiction!

- Intuitive solution: build a macromodel for sensitive region
  - It’s recently proposed with a FDM based implementation [1]
  - The used macromodeling technique was created many years ago for reducing the runtime for large structure [2]

Notice: the macromodeling technique has not been utilized by the state-of-the-art FRW based capacitance solver.

The aim of this work:
- Combine macromodeling and FRW techniques, to improve the capacitance field solver for several scenarios.

Major contributions:
- A new random walk algorithm which utilizes the macromodel and is able to handle general 3-D layout.
- Handle the capacitance extraction with encrypted structures, while keeping the advantages of FRW method.
- We also propose to apply it to problems with complex geometry and repeated layout patterns, for extending FRW’s capability and improving its runtime efficiency.
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Technical Background – FRW method

- Integral formula for electric potential
  \[ \phi(r) = \int_{S_1} P_1(r, r^{(1)}) \phi(r^{(1)}) \, dr^{(1)} \]

  Surface Green’s function \( P_1 \) can be regarded as a probability density function.

- Monte Carlo method: \( \phi(r) = \frac{1}{M} \sum_{m=1}^{M} \phi_m \)
  \( \phi_m \) is the potential of a point on \( S_1 \), randomly sampled with \( P_1 \).

- How to do if \( \phi_m \) is unknown? expand the integral recursively
  \[ \phi(r) = \int_{S_1} P_1(r, r^{(1)}) \int_{S_2} P_1(r^{(1)}, r^{(2)}) \cdots \int_{S_k} P_1(r^{(k-1)}, r^{(k)}) \phi(r^{(k)}) \, dr^{(k)} \cdots dr^{(2)} \, dr^{(1)} \]

This spatial sampling procedure is called floating random walk.
A 2-D example with 3 walks

- Use maximal cube transition domain

How to calculate capacitances?

\[
\begin{bmatrix}
C_{11} & C_{12} & C_{13} \\
C_{12} & C_{22} & C_{23} \\
C_{13} & C_{23} & C_{33}
\end{bmatrix}
\begin{bmatrix}
V_1 \\
V_2 \\
V_3
\end{bmatrix}
= \begin{bmatrix}
Q_1 \\
Q_2 \\
Q_3
\end{bmatrix}
\]

\[Q_1 = C_{11}V_1 + C_{12}V_2 + C_{13}V_3\]

Integral for calculating charge (Gauss theorem)

\[Q_1 = \oint_{G_1} F(r) \cdot \hat{n} \cdot \nabla \phi(r) \, dr = \oint_{G_1} F(r) \cdot \hat{n} \cdot \nabla \int_{S_1} P_1(r,r^{(1)}) \phi(r^{(1)}) \, dr^{(1)} \, dr\]

\[= \oint_{G_1} F(r) g \oint_{S_1} P_1(r,r^{(1)}) \phi(r^{(1)}) \omega(r,r^{(1)}) \, dr^{(1)} \, dr\]

weight value, estimate of \(C_{11}, C_{12}, C_{13}\) coefficients

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Technical Background – FRW method

- Make random sampling with \( P_1 \) probability function
  - Available for cube transition domain
  - Pre-calculate the probabilities from center to surface panels (GFT)
  - \( \omega(r, r^{(1)}) \) is also pre-calculated (WVT)

- Keys of fast FRW algorithm for Manhattan geometry
  - GFT/WVTs for cubic transition domain are critical for performing fast sampling
  - Large probability to terminate a walk; easy to design a spatial structure for fast calculation of distance [4]
  - Techniques for handling multiple planar dielectrics

- Runtime of FRW: \( T_{total} = N_{walk} \cdot N_{hop} \cdot T_{hop} \)

The idea of macromodel for capacitance extraction
- Built for a sub-structure in problem domain
- A matrix reflecting electrostatic coupling
- Built with FDM or BEM, originally for global hierarchical extraction [5][2]

Two different definitions
- Boundary potential-flux matrix (BPFM): \( \mathbf{A} \mathbf{u} = \tilde{\mathbf{q}} \)
  \( \mathbf{u} \) and \( \tilde{\mathbf{q}} \) are vectors of potential and normal electric field intensity on the boundary elements. [5][2]
- Boundary potential-charge matrix (BPCM): \( \mathbf{C} \mathbf{u} = \mathbf{q} \)
  \( \mathbf{q} \) is vector of electric charge. Called Markov transition matrix [6]

We use BPCM \( \mathbf{C} \leftrightarrow \) Capacitance matrix for a closed-domain

The fabric-aware capacitance extraction problem [6]

- Simulated structure: a combination of predefined motifs
- Motif positions topologically vary
- A hierarchical random walk method pre-calculates BPCM for each motif, and then performs Markov chain RWs among boundary elements/conductors

On the interface of motifs

\[ Q_i = \left( -C_{ii}^{(1)} \right) \sum_{j=1, j \neq i}^{N_1} \left[ \frac{C_{ij}^{(1)}}{C_{ii}^{(1)}} U_j^{(1)} \right] \]

\[ U_k = \sum_{j=1, j \neq k}^{N_1} \left( -C_{kj}^{(1)} \right) \left[ \frac{C_{kk}^{(1)} + C_{kk}^{(2)}}{C_{kk}^{(1)} + C_{kk}^{(2)}} U_j^{(1)} \right] + \sum_{j=1, j \neq k}^{N_2} \left( -C_{kj}^{(2)} \right) \left[ \frac{C_{kk}^{(1)} + C_{kk}^{(2)}}{C_{kk}^{(1)} + C_{kk}^{(2)}} U_j^{(2)} \right] \]

\[ C^{(1)} \sim \text{a capacitance matrix} \]

...they are probabilities for random transition

**No geometry computation. So, MCRW runs faster than FRW!**

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A general structure partially described by macromodels

- MCRW doesn’t work

The new algorithm

- Idea: Use a patch region to combine MCRW for a sub-structure with macromodel + FRW for the structure elsewhere
- If we have the macromodel for the patch, MCRW works for sub-structure’s boundary point
- Then, if the walk position is out of sub-structure, the FRW is feasible
- This blank patch region can be scaled in size, with its macromodel reusable

\[
\frac{1}{l'} C' = \frac{1}{l} C
\]
The benefits of this new algorithm
- Solve the structure encryption problem in FRW-based extr.
- Extend capability and improve efficiency

Some details
- Patch region = half a cube
- Easy to find the largest patch (similar to finding the largest transition cube in FRW)
- Walk point always corresponds to same local index in patch’s macromodel, only one row of BPCM is needed
- A new MCRW formula for the mismatched interface discretization

\[
U_k = \sum_{j=1, j \neq k}^{N_1} \frac{-C_{kj}^{(1)}}{A_k^{(1)}} U_j^{(1)} + \sum_{j=1, j \neq k}^{N_2} \frac{-C_{kj}^{(2)}}{A_k^{(2)}} U_j^{(2)}
\]
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Capacitance Extraction Applications

- Three kinds of applications
  - Encryption of sensitive structure
    - Foundry/IP vendor build macromodel for a sensitive region, avoid presenting its details to EDA vendor/IC designer
    - Memory cost depends on the quantity/size of such regions
  - Handling complex sub-structure
    - Select a sub-region including complex geometry feature, and make macromodel
    - Extend the capability of FRW method
    - Useful for digital circuit with minor complex features
  - Circuit w/ repeated layout patterns
    - Memory IC or FPGA
    - Reduce memory for storing layout
    - Accelerate the capacitance extraction
Numerical Results with 3-D Test Cases

- **Experiment setup**
  - All random walk programs terminate with 0.5% 1-σ error
  - Macromodels are built with BEM; data size for the patch is 162KB/1.5MB for single/multi-dielectric cases
  - Serial computing on Xeon 2.0GHz CPU

- **Encryption of sensitive structure**
  - **Case 1**: 3x3 crossover above a FinFET
  - **Case 2**: two FinFET black boxes

<table>
<thead>
<tr>
<th>Test case</th>
<th>RWCap2$^{[4]}$</th>
<th>The proposed method</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$N_{\text{walk}}$</td>
<td>$N_{\text{hop}}$</td>
</tr>
<tr>
<td>1</td>
<td>351K</td>
<td>39.5</td>
</tr>
<tr>
<td>2</td>
<td>161K</td>
<td>37.4</td>
</tr>
</tbody>
</table>

8.2MB data size for macromodeling the FinFET black box

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Numerical Results with 3-D Test Cases

- Handling complex sub-structure
  - **Case 3**: include conformal dielectric
  - **Case 4**: a 45°-angle bevel wire above a 3x3 crossover
- Set a mid-layer conductor as master

<table>
<thead>
<tr>
<th>Test case</th>
<th>Raphael</th>
<th>The proposed method</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>C(aF)</td>
<td>N_{walk}</td>
</tr>
<tr>
<td>3</td>
<td>66.14</td>
<td>370K</td>
</tr>
<tr>
<td>4</td>
<td>47.68</td>
<td>152K</td>
</tr>
</tbody>
</table>

The slightly larger error for Case 3 may be caused by different outer-boundary condition in Raphael RC3

- The sub-structures in Case 3, 4 cost 7.1MB and 45MB macromodel data; building time is 2.87s and 24.1s
- Cost may be amortized for extraction with multiple masters
Circuit with repeated layout patterns

- **Case 5**: 8x8 duplication of a structure pattern in M1 layer
- Set different conductors as master

2.7s and 6.4MB data are needed for macromodeling

If the master is within a cyclic pattern, the proposed method can be > 10X faster than FRW

Markov Chain RW makes $N_{walk}$ largely reduced

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**Numerical Results with 3-D Test Cases**

<table>
<thead>
<tr>
<th>Case 5 master</th>
<th>RWCap2$^{[4]}$</th>
<th>The proposed method</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$N_{walk}$</td>
<td>$N_{hop}$</td>
</tr>
<tr>
<td>Con1</td>
<td>217K</td>
<td>27.7</td>
</tr>
<tr>
<td>Con2</td>
<td>577K</td>
<td>14.1</td>
</tr>
<tr>
<td>Con3</td>
<td>286K</td>
<td>35.2</td>
</tr>
</tbody>
</table>

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Conclusion

• The Markov chain random walk and the floating random walk are combined to accelerate the capacitance extraction, and handle circuits including IP protected or geometry-complex sub-structures

• The scalable blank patch region: with it and its macromodel, we can establish a general & accurate macromodel-aware extraction algorithm

• It extends the capability of the state-of-the-art FRW based capacitance solver with negligible overhead

• It can bring over 10X speedup to the FRW based extraction for circuit with repeated layout patterns
References

The Floating Random Walk Algorithms for Capacitance Extraction Problems in IC and FPD Design:

References


- My Homepage:
- [http://numbda.cs.tsinghua.edu.cn](http://numbda.cs.tsinghua.edu.cn)
Thank You!